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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,020	12/20/2000	Christopher B. Wilkerson	884.370US1	8132

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EXAMINER

INOA, MIDYS

ART UNIT	PAPER NUMBER
2188	3

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/745,020

Applicant(s)

WILKERSON, CHRISTOPHER B.

Examiner

Midys Inoa

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 December 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 20th, 2000 has been considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: distributed memory machine 700. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 17 and 18 are objected to because of the following informalities:

The word "to" between the words "identifiers" and "indicate" should be deleted. The phrase should read: "plurality of identifiers indicate".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 4, 5, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Improving Data Cache Performance by Pre-

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executing Instructions Under a Cache Miss” by James Dundas and Trevor Mudge (Dundas et al.) in view of Ukai et al. (5,983,324).

Regarding Claims 1 and 12, Dundas et al. teaches a technique for improving data cache performance by pre-executing future instructions under a data cache miss (“run-ahead execution”, Abstract). Dundas et al. does not teach setting a protection bit associated with the data that was pre-executed, thus protecting it from eviction prior to its use. Ukai et al. teaches a prefetch method which suppresses replacement of prefetched data (through means of protection settings) by other data before the prefetched data is used (Column 2, lines 47-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the prefetch method of Ukai et al. with the Pre-execution method of Dundas et al. since both methods perform a type of prefetching operation and integrating the method of Ukai to Dundas’ Pre-execution method would Pre-executed data from being lost before it is put to use.

Regarding Claims 4-5 and 13, Ukai et al. teaches protecting only prefetched data. Therefore, it is understood that during normal execution (when prefetching is not occurring) all protection parameters should be cleared, especially once prefetched data is put to use during normal execution. In addition, before prefetching begins again, all protection parameters should be cleared since there should be no prefetched data already stored in the cache.

Regarding Claims 14-15, prefetching algorithms are known to be implemented reliably in software, therefore, it would be understood if such software implementation would come directly from a specific section in a program. In addition, since some software programs need to be compiled prior to their execution, it is understood that a prefetching algorithm may too come from a compiler.

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Regarding Claims 16, 21, and 25, Dundas et al. teaches a technique for improving data cache performance by pre-executing future instructions under a data cache miss ("run-ahead execution", Abstract). Dundas et al. does not teach setting a protection bit associated with the data that was pre-executed, thus protecting it from eviction prior to its use. Ukai et al. teaches a prefetch method employed in a cache system where a cache area with a plurality of lines may load target data ("data to be executed") to an user buffer in the processor ("plurality of registers") in order for the processor to access it (Figure 1). The prefetch method of Ukai suppresses replacement of prefetched data in the cache (through means of protection settings) by other data before the prefetched data is used (Column 2, lines 47-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the prefetch method of Ukai et al. with the Pre-execution method of Dundas et al. since both methods perform a type of prefetching operation and integrating the method of Ukai to Dundas' Pre-execution method would Pre-executed data from being lost before it is put to use.

Regarding Claims 17 and 18, the protection mechanism disclosed by Ukai et al. acts a identifier since it indicates that the data is prefetch data that has yet to be used by the processor.

Regarding Claims 19 and 24, some caches are known to have cache directories (or tag arrays), which normally hold detailed metadata information such as address tag information, hit/miss information, and protection bits.

Regarding Claims 20, 22, and 23, cache controllers are known to use metadata information (such as protection bits) held in cache directories to control the function of the cache.

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Regarding Claims 26-28, the Pre-execution and protection method of the invention is described as to work for any cache in any computer system. Therefore, it is understood that such method could be used in an L1 cache, an L2 cache or an on die cache.

6. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dundas et al. in view of Ukai et al. as applied to claim 1 above, and further in view of Petrick et al.

(5,920,889). The combination of Dundas et al. in view of Ukai et al. does not teach evicting a cache line in order to store the pre-executed (or prefetched) data into the cache. Petrick et al. teaches a prefetch method in which a cache line is evicted from the cache in order to make room for prefetched data (Column 5, lines 46-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the eviction policy of Petrick et al. with the invention portrayed by the combination of Dundas et al. and Ukai et al. since adding this policy would ensure that the cache always has room to receive the pre-executed data. In performing this eviction policy within the invention of Dundas et al. in view of Ukai et al. the Pre-execution method would evict a line from the cache, store the Pre-executed data in such cache line, and protected from being prematurely evicted.

7. Claims 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dundas et al. in view of Ukai et al. (5,983,324) and further in view of Petrick et al. (5,920,889).

8. Regarding Claims 6, 7, 9, and 10, Dundas et al. teaches a technique for improving data cache performance by pre-executing future instructions under a data cache miss ("run-ahead execution", Abstract). Dundas et al. does not teach setting a protection bit associated with the data that was pre-executed, thus protecting it from eviction prior to its use. Ukai et al. teaches a prefetch method which suppresses replacement of prefetched data (through means of protection

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settings) by other data before the prefetched data is used (Column 2, lines 47-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the prefetch method of Ukai et al. with the Pre-execution method of Dundas et al. since both methods perform a type of prefetching operation and integrating the method of Ukai to Dundas' Pre-execution method would Pre-executed data from being lost before it is put to use. The combination of Dundas et al. in view of Ukai et al. does not teach evicting a cache line in order to store the pre-executed (or prefetched) data into the cache. Petrick et al. teaches a prefetch method in which a cache line is evicted from the cache in order to make room for prefetched data (Column 5, lines 46-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the eviction policy of Petrick et al. with the invention portrayed by the combination of Dundas et al. and Ukai et al. since adding this policy would ensure that the cache always has room to receive the pre-executed data. In performing this eviction policy within the invention of Dundas et al. in view of Ukai et al. the Pre-execution method would evict a line from the cache, store the Pre-executed data in such cache line, and protected from being prematurely evicted.

Regarding Claims 8 and 11, Ukai et al. teaches protecting only prefetched data. Therefore, it is understood that during normal execution (when prefetching is not occurring) all protection parameters should be cleared, especially once prefetched data is put to use during normal execution. In addition, before prefetching begins again, all protection parameters should be cleared since there should be no prefetched data already stored in the cache.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Midys Inoa
Midys Inoa
Examiner
Art Unit 2188

MI

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9/30/03

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TC 2100